Function Feature

It is compatible with both three-phase three-wire and three-phase four-wire.

High accuracy electrical energy measurement. It matches IEC678/6103 GB/T 1721 and IEC1268 GB/T 17882.

The error of active electrical energy measurement is less than 0.1% in the dynamic area 1000:1.

The error of reactive electrical energy measurement is less than 0.2% in the dynamic area 1000:1.

It can accurately measure the reactive electrical energy of up to 21st harmonic.

Active/reactive calibration meter pulse output

Measuring instantaneous active/reactive, line voltage frequency and RMS value of voltage/current.

Simultaneously supply split phase and mergence phase active/reactive and symbolic indication

It can select energy accumulation mode of mergence phase (algebra summation/absolute value summation)

Two stepping motor drive output, which can simultaneously output active/reactive power

Lose of phase/ under-voltage/ over voltage detecting, it has interrupt output.

Current channel embeds Programmable Gain Amplifier (PGA).

Support digital phase correction and linear compensation of small current segment

Built-in digital temperature sensor, support segment compensation of temperature

Constant of electrical energy meter and starting current can be calibrated by digit.

SPI interface, which facilitate control of external microprocessor.

AD waveform data of real time voltage and current of all phases

Temperature standard of industry class, QFP44 pin packaging.

Description of the functions

PL3223 is a high accuracy, multifunctional three-phase electrical energy measurement chip, which support SPI interface and power pulse output, and has self-defining frequency division ratio wheel-drive pulse output. PL3223 integrates second-order - ADC, which refer to voltage source, temperature sensor, power source detecting, all active/reactive electrical energy measurement and voltage/current RMS value, and digital signal processing module measured by line voltage frequency.

Pl3223 supports active and reactive measurement in different electrical networks, such as three-phase three-wire system, three-phase four-wire system. Furthermore, it is compatible with frequency of different electrical networks. It can realize high accuracy measurement of power in the electrical networks of 50Hz standard and 60Hz standard frequency.

PL3223 not only supplies real time information of active power and reactive power through pulse output pin PCF and QCF, but also provides RMS value of voltage and current, and measurement function of line voltage frequency. (read by built-in registers VRMS(34 37H) and IRMS(38 3BH)) User can obtain apparent power through calculating RMS value of voltage and current.

PL3223 embeds eight 8-bit counters of three-phase/mergence-phase active/reactive power pulse, which is used to assist the pulse count of external MCU. As a result, the problem of losing pulse-count can be completely solved.

PL3223 supports resistance network collation of self-defining frequency division. Meanwhile, it supplies full digital correcting function. PL3223 supplies 13 correcting registers to calibrate output threshold of active power, output threshold of reactive power, three-phase active/reactive gain compensation, and three-phase phase compensation. PL3223 can combine with monolithic computer to fulfill effective precise calibration.

PL3223 supports over voltage of line voltage, under-voltage detecting function, and shooting interrupt signal as caution when voltage happens abnormity. Through over voltage/under-voltage peak value register and under-voltage half period number register, user can set up the conditions producing early warning signal by self-definition method.

PL3223 conducts data communication with external CPU through SPI interface. Interrupt signal of PL3223 is a logical output signal which low level is effective. When one phase or more phases appear over voltage/under-voltage abnormity situation, PL3223 shoots interrupt signal. Through reading voltage monitoring register FLAG (29H), CPU can judge what phase appear abnormity situation and what abnormity situation is happening. Meanwhile, it can also obtain the range of duration of voltage abnormity by real time monitoring FLAG.

PL3223 can read real time waveform of three-phase voltage and current through SPI interface so that user can easily analyze harmonic;

PL3223 needs to link 9.6M external crystal oscillator or clock input;

PL3223 supplies 44-lead QFP packaging.

# FXXC®
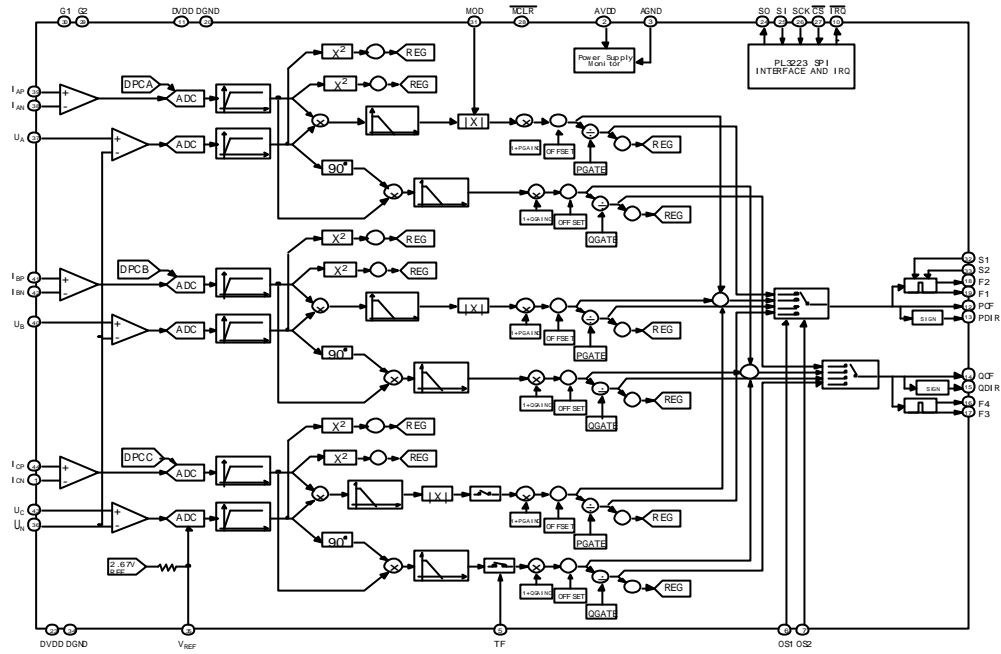
PL3223

Specification Introduction

AVDD=DVDD=5V± 5%   AGND=DGND=0V   clock input=9.6MHz   built-in voltage benchmark

Parameter	Specification	Unit	Testing conditions/explanation
Precision Measurement error of active electrical energy	<0.1%		
Analog input			
Maximal input level	±350	mV Peak to Peak	
Input impedance DC	200	kO min	
Bandwidth -3dB	10	kHz typ	
ADC detuning error	30	mV max	
Gain error	±8	% typ	Exterior 2.5V voltage benchmark
Gain error matching	±3	% typ	Exterior 2.5V voltage benchmark
Reference voltage input			
REFIN/OUT input voltage arrange	2.4	V max	
	2.1	V min	
Input impedance	2.1	kO max	
Input capacitance	12	pF max	
Embed ded Voltage benchmark			
Benchmark source error	±200	mV max	
Temperature coefficient	30	ppm/ typ	
Temperature sensor	±4		
Block input			
Input block frequency	9.6	MHz typ	
Logic input			
Input high level VINH	2.4	V min	DVDD = 5V±5%
Input low level VINL	0.8	V max	DVDD = 5V±5%
Input current IIN	±3	uA max	VIN = 0V - DVDD
Input capacitance CIN	10	pF max	
Logic output			
Output high level VOH	4	V min	DVDD = 5V±5%
Output low level VOL	1	V max	DVDD = 5V±5%
Power supply			
AVDD	4.75	V min	
	5.25	V max	
DVDD	4.75	V min	
	5.25	V max	
AIDD	7	mA max	
DIDD	18	mA max	

PL3223

SPI Sequential Character Table

| Parameter	Specification	Unit	Notes
Write sequential			
t1	200	ns (min)	CS falling edge to the first leading edge of SCK
t2	200	ns (min)	SCLK high level pulse width
t3	200	ns (min)	SCLK low level pulse width
t4	10	ns (min)	Time effective data reach before SCK leading edge
t5	5	ns (min)	Time effective data retain after SCK leading edge
t6	200	ns (min)	Minimal transmission time of data byte
t7	300	ns (min)	Time CS retains after SCK leading edge
Read sequential t8	100	ns (min)	Effective time of data output after SCK falling edge
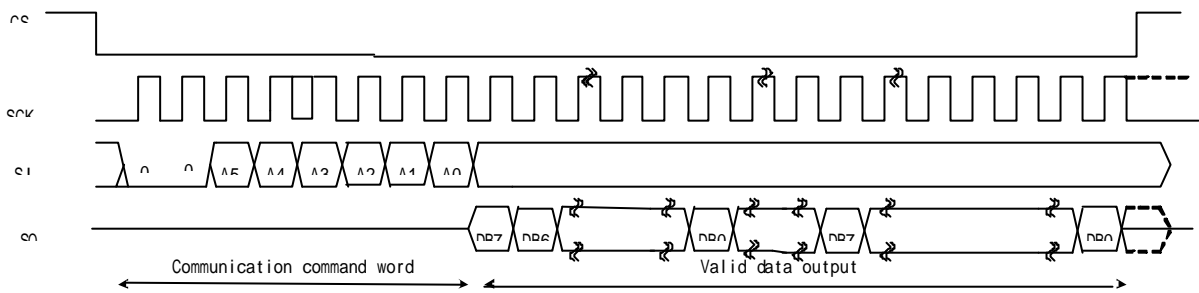
SPI sequential figure of read operation
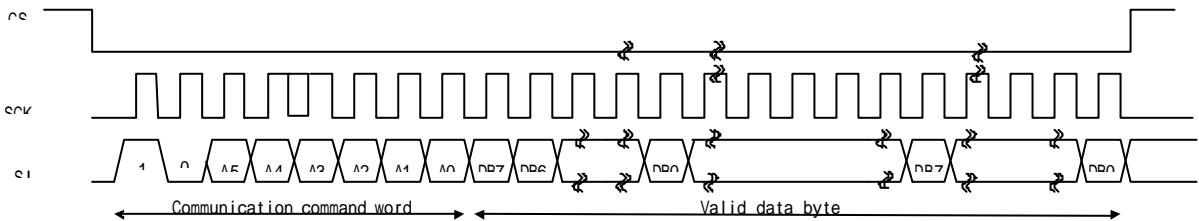
SPI sequential figure of write operation

Limiting Parameter   TA=+25

AVDD to AGND . . . . -0.6V to +7V

DVDD to DGND . . . . -0.6V to +7V

DVDD to AVDD . . . . -0.6V to +0.6V

Analog Input Voltage to AGND

   IAP,IAN,IBP,IBN,ICP,ICN,UA,UB,UC, UN . . . . -0.6V to AVDD + 0.6V

  Refference voltage input to AGND . . . . -0.6V to AVDD + 0.6V

  Logic input voltage to DGND . . . . -0.6V to DVDD + 0.6V

  Logic output voltage to DGND . . . .-0.6V to DVDD + 0.6V

Work temperature range   Industry grade   . . . . -40   to +85

Storage temperaure arrange . . . . -65   to +150

ESD protection 3000V

Junction temperature. 150

Pin welding temperature 215   45sec

Packaging Form (44-Lead QFP)
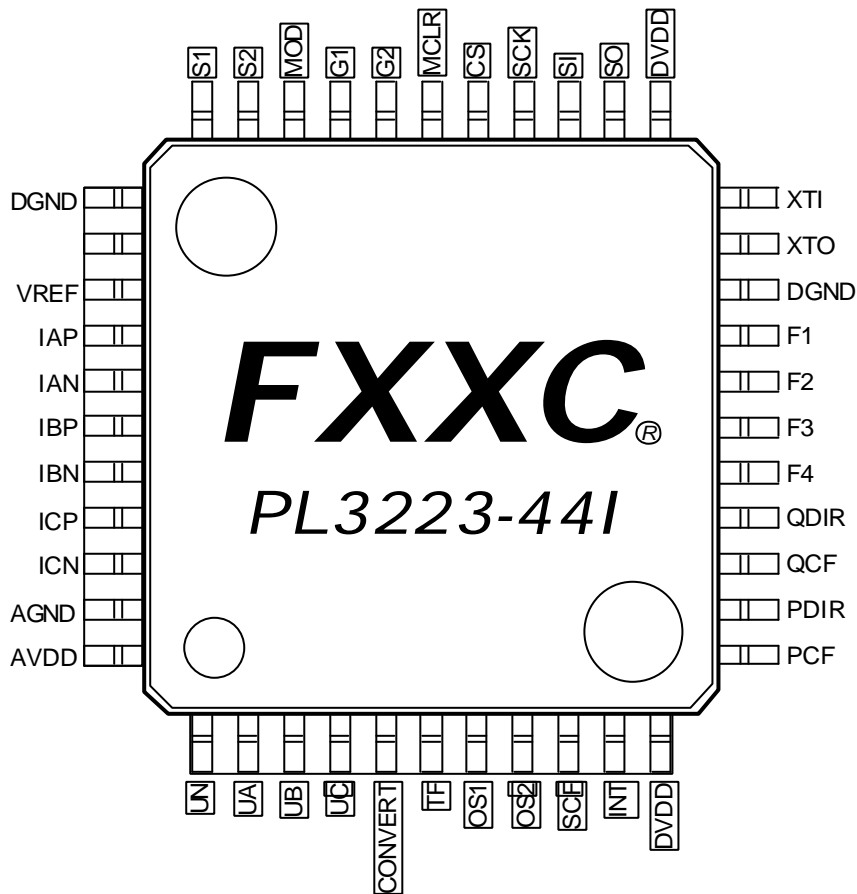
Sketch map of pin distribution of PL3223

PL3223

Description of functions of pins

Pin Number	Mnemonic Symbol	Detail Description
1 2 3 4	UN, UA, UB, UC	Voltage channel analog signal input
5	CONVERT	AD sampling indication signal low level is valid frequency is 5kHz.
6	TF	Three-phase three-line/three-phase four-line working mode option. 0 is three-phase four-wire 1 is three-phase three-wire In the mode of three-phase three-wire, only channel A and B work, the channel C is in the situation of stop
7 8	OS1 OS2	Separated phase/combined phase output option separated phase output is used for testing of calibrating meter for setting detail, please see page 11.
9	SCF	Dividing frequency setup of power pulse and wheel driving pulse, for setting details, see page 13.
10	IRQ	Over voltage/under-voltage interrupt output low level pulse
11, 23	DVDD	They connect 5V power supply of digital part. 10uF and 0.1uF decoupling capacitance should be set between they and DGND.
12	PCF	Active instantaneous pulse output high level is valid which is used for testing of calibrating meter.
13	PDIR	Indication of symbol bit of active instantaneous power
14	QCF	Reactive instantaneous pulse output high level is effective which is used for testing of calibrating meter.
15	QDIR	Indication of symbol bit of reactive instantaneous power
16, 17	F4, F3	Stepping drive of reactive energy cumulative indicator two phase/two beats wheel
18, 19	F2, F1	Stepping drive of active energy cumulative indicator two phase/two beats wheel
20, 34	DGND	Connect to power supply earth of digital part
21, 22	XTO, XTI	Reversed phase output/input interface of embedded oscillator can link 9.6Mhz external crystal oscillator or clock input . In the case of using crystal oscillator, link 22 to 33pF external capacitance.
24	SO	SPI four wire data output of interface series shift
25	SI	SPI four wire data input of interface series shift
26	SCK	SPI four wire synchronous clock input of interface series
27	CS	SPI four wire interface chip-selection input low level is effective
28	MCLR	External manual reset low level reset
29, 30	G2, G1	Option input of gain of current channel PGA, usually be advised to link earth. setting detail see page 6.

PL3223

31	MOD	Summation mode option of combined phase electric energy 0 is algebra summation 1is summation of absolute value
32, 33	S2, S1	Power pulse and dividing frequency setup of pulse of wheel driving, setting detail see page 13
35	NC	Empty pin
36	VREF	Embedded voltage benchmark source output/external voltage benchmark resource input. This pin should 1uF capacitor should be set between this PIN and AGND
37, 38 39, 40 41, 42	IAP, IAN IBP, IBN ICP, ICN	Analog signal input of current channel
43	AGND	Connect to power supply earth of analog part
44	AVDD	Connect 5V power supply of digital part 10uF and 0.1uF decoupling capacitor should be set between this PIN and AGND

PL3223

Description of PL3223 Principle

Detecting of Power Failure

PL3223 has the monitoring module of power supply, which serially monitors voltage value of pin AVDD of analog power supply. When voltage value is less than 4.75V PL3223 shall automatically enter reset state and stop any normal functions. This character can make the chip fulfill self-protecting in the case of electrifying or power failure of power supply. Power detecting module has Schmidt trigger circuit character. Thus, power supply noise shall not cause abnormal reset

Analog Input

PL3223 has six input interface of analog signals. Thereinto, input pins of three pair of difference signals compose current signal interfaces [IAP, IAN], [IBP, IBN], [ICP, ICN]. When use inside reference source and PGA is × 4, the maximal difference signal input can be converted is peak to peak± 350mV

Voltage signal input is composed by three single-interface voltage input pins VAP, VBP, VCP and one reference neutral point input pin VN

Compare with current input, there is a similar situation. The range of difference signal input of VAP, VBP, VCP is peak to peak ± 350mV to VN

Current signal channel has PGA (controllable gain) control function. It can set up amplification factor of PGA through setting level of pins G1, G2 30, 29 Usually this PGA gain multiple does not need to be changed. It is advised the setup is 00 namely × 4 state However, user also can connect pins of G1 and G2 to output pins of single-chip and then according to plate design, set self-defining suitable amplification multiple by single-chip software so that size of input signal is suitable for the arrange of AD converting, It should be paid attention that the maximal input shall change too at the same time.

Relationship between level of G1 and G2 and PGA amplification multiple (See table below)

G2	G1	PGA Gain Multiple
0	0	× 4 (Default)
0	1	× 8
1	0	× 16
1	1	× 32

Reference Voltage

PL3223 supplies a built-in stabilized voltage power supply for AD as the reference voltage of converting. The reference level supplied is about 2.1V. Usually user does not need to link external reference voltage resource.

Modulus converts module

PL3223 has six 16bit second-order ADC type of ADC need to pay the expense of increase over sampling frequency in order to gain higher precision. The principle predigested is displayed in chart 1. type of ADC is composed by the part of analog modulation of the front and the part of digital filter of back end. ADC of PL3223 outputs sampling data of 5K rates, which are provided to signal processing unit for calculating power. User also can read them from SPI interface.
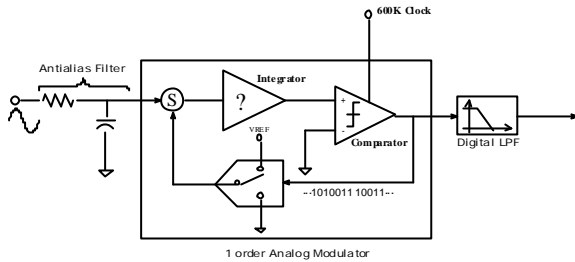
figoure1 first order   type ADC principle chart

type of ADC converts input signals to 1bit series data which composed by 1 and 0. The data rate is 1/16 600K of main clock in PL3223. If difference signal voltage of input is in the range of reference voltage, there is a corresponding and directly proportional relationship between the average value of series data and level value of input signal. Any one independent data of the series data is insignificant. The significant result only can be obtained through averaging much series data. This is the function of digital low pass filter of ADC. Through digital low pass filter, 1bit 600k series data are converted into 16bit/5kHz numerical value so as to complete the conversion from analog signal to digital signal.

The key factor that   type of ADC can gain high resolution sampling is pass sample, namely sample rate more bigger than useful signal bandwidth need to convert. For example, Sample rate of PL3223 is 600kHz signal bandwidth of voltage and current need to convert is from 40Hz to 2.5kHz. See chart 2 Pass sample shall expand quantization noise to a very broad spectral range. However, the quantization noise energy of low frequency part includes useful signal is very less. This result is caused by integrator of modulator. It benefits to use digital low pass filter filtering noise so that gain useful signals have high signal to noise ratio.
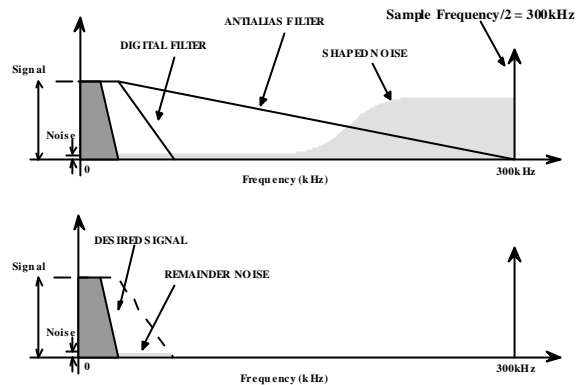

Chart   2 Sketch map of frequency domain of type of ADC

Interior Register of 3223

PL3223 has 38 interior function registers. The details of functions are showed in the appendix1 <PL3223 register list>. The registers conduct reading and writing operation through SPI.

Interior registers are protected after PL3223 is electrified. If it wants to conduct writing operation to registers, it is necessary to cancel write protection firstly. The method is to write 1byte data FF to address 3F. After canceling of write protection, registers are under write state. When user writes 1 byte date 00 to address 3F, write protection is available again. Here, write operation of registers is not available. In order to ensure registers are not changed, we advise that write protection is set as availability after finishing write operation of SPI.

The point needs to be paid attention: When starting up frequency measurement or current/voltage RMS value measurement, it is necessary that writing 1byte data to read-only register 30H for starting up measurement process. Here, we do not need to cancel write protection. It is also available.

PL3223

AD User Interface of **3223**

PL3223 can directly read AD data of three-phase voltage and current through interior registers. The method is that writing 1byte data to register SEL_CH 1CH to appoint voltage access need to be measured. 1 is A phase 2 is B phase 3 is C phase PL3223 indicates AD conversion state through pin CONVER. Pin CONVERT outputs pulse signal of 5K frequency under normal state. CONVERT is set low for once means finish of AD conversion for once. User can use CPU to respectively read 2bytes voltage and current data from address 2C~2DH and 2E~2FH through SPI.

Frequency Measurement

PL3223 adopts embedded pass zero detecting technology to supply frequency measurement function of line voltage. Before measuring frequency, user firstly need to write data to register SEL_CH 1CH to appoint voltage access need to measure. 1 is A phase 2 is B phase 3 is C phase Then conducts one write operation to read-only address 30H through SPI, namely write any 1byte data such as 00. Here, frequency measurement function is started up. After startup, PL3223 enters the state of frequency and RMS value measurement. Here, the functions of active/reactive measurement and the other are in the normal work state.

PL3223 shall measure the time that serially appear 50 times and positive pass zero. Thus, once of frequency measurement will last at least 1 second for line voltage of 50Hz frequency. From waiting for enough time to completing all measurement, 2bytes data is read out from register DFC (30H, 31H). The data usually is about 5000 of decimalization in the case of 50Hz line voltage. Line voltage

frequency can be obtained by the result that 250,000 divide this data.

Measurement of RMS Value of Voltage and Current

PL3223 provides information of RMS value of current line voltage and line current through a simplified RMS value measurement unit. PL3223 does not provide exact Root-Mean-Square value of voltage and current. It provides square accumulating value in a fixed period. User reads out this square accumulating value and divide total amount of samples, and then extract it. The result is the RMS value of line voltage and line current. The detail steps are similar to frequency measurement: Firstly write data to register SEL_CH 1CH to appoint voltage access need to be measured 1 is A phase 2 is B phase 3 is C phase. Then write 1byte any data such as 00 to 30H start up RMS value measurement function. During the time of measuring RMS value PL3223 measures time serially appear 14 times and positive pass zero. Thus, time of once of RMS value measurement will last at least 280ms for line voltage of 50Hz frequency. From waiting for enough time to completing all measurement, 4bytes of square integrated value of line voltage is read out from register VRMS 34H 37H . 4bytes of square integrated value of line current is read out from register IRMS 38H 38H . 2bytes of sample points value is read out from M_CNT 3CH 3DH . RMS value of Line voltage/current can be obtained by calculating the result that square integrated value divides sample point number and then extract it,

Namely,

$$V_{RMS} = \sqrt{VRMS / M\_CNT}$$
$$I_{RMS} = \sqrt{IRMS / M\_CNT}$$

Monitoring of Voltage

PL3223 has the function of voltage monitoring, which can raise caution when happen abnormal phenomenon. User can flexibly configure conditions of voltage monitoring through over voltage valve value, under-voltage valve value and under-voltage half circle wave number of self-defining parameters of user.

It is different to judge over voltage and under-voltage in PL3223. While instantaneous voltage value of any one phase over the over voltage valve value defined, PL3223 immediately judges this is an over voltage event and will raise the alarm interrupt at the end of period. On the other hand, when any instantaneous voltage value pass zero twice does not reach the under-voltage valve value defined, PL3223 does not immediately judge this is an under-voltage event. It only records the continuous half cycle number. Once serial under-voltage time over half circle wave number defined, it judges this is an under-voltage event, and raise the alarm interrupt. We choose the different processing ways is because there is different potential dangerous degree between over voltage and under-voltage.

PL3223 monitors three-phase voltage value at the same time. When any one phase happens abnormal phenomenon, IRQ 10 pin raises low effective caution interrupt which pulse width is 1.5ms.   After receiving the caution interrupt, user may read the state of FLAG 29H   to know which phase appears abnormal phenomenon and what kind of abnormity is happening. The status word of state indication register renews once every voltage period.

PL3223 generates caution interrupt when abnormal cases appear only. It does not

generate interrupt again when voltage recover to normal state from abnormal state. The status word of state indication register always displays real-time running state of electric network voltage. Thus, user may know about time that abnormal phenomenon of voltage lasts through the way of checking in turn.
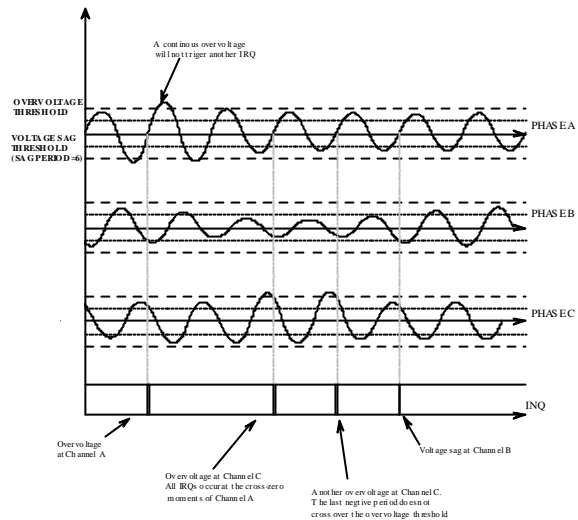

Chart 3 Example of three-phase over voltage and under-voltage

INT_ENA   1BH   can configure whether interrupt is made for three-phase over voltage/under-voltage. PL3223 closes all of interrupt function in the state of electrifying default. It needs to be emphasized that over voltage/under-voltage state register FLAG is not affected by interrupt function register. For example, through defining function, phase A over voltage interrupt is forbidden. When A phase voltage happens over voltage, bit4 of FLAG still become "1". However, there is no interrupt here.

For facilitating user to set up rational over voltage   and   under-voltage   valve   value, PL3223 provides function of peak value voltage measurement. User may measures current peak value voltage value after knowing about electric network is normal. And based on this voltage value, we can calculate over

voltage valve value and under-voltage valve value that need to configure, and conduct configuration, The register of configuring over voltage valve value is 18H, The register of configuring under-voltage valve value is 19H

The way of measuring peak value voltage is similar to frequency measurement and RMS value measurement. Firstly, use access option register SEL_CH 1CH to select voltage access need to be measured, write 1 as A phase 2 is B phase 3 is C phase Then write 1byte any data such as 00 to 30H start up function of peak value measurement, after waiting for two voltage period, read 2bytes data from address 32H~33H . This is voltage peak value expressed by 2tytes. After gaining voltage peak value of normal state, we can get over voltage valve value and under-voltage valve value that need to be configured through calculating. The way is high byte multiply corresponding proportion. Notice: In the case of three-phase three-line mode TF 1 , PL3223 still can fulfill voltage monitoring. Here, voltage channels of A phase and B phase are monitored (namely, two line voltages that user links exterior) C phase voltage channel is shielded. Under-voltage indication of C phase of over voltage/under-voltage state register maybe is high, but no interrupt----no matter interrupt function of C phase is opened or not.

Active Measurement

Active electric energy may be viewed as energy stream which flows to load from power supply in physics. "Speed" user consumes electric energy at a certain time is called instantaneous power. It equals the product of instantaneous voltage value and instantaneous current value at this time in

mathematics. Total consumption amount of electric energy of user equals sum of all of these "instantaneous" electric energy consumed. As a result, calculation of active electric energy is integral of product of voltage and current instantaneous value to time. See (1)

$$E = \int P dt = \int u i dt \qquad (1)$$

To the alternating current that voltage and current are sine signals, 1 equal following form

$$E = \int P dt = \int U I \cos f dt \qquad (2)$$

Thereinto, *U,I respectively are 0.707 magnitude of AC voltage and current signal* they are called AC RMS value. f is phase difference value that voltage signal over current signal $\cos f$ is called power factor. It expresses ratio of product (apparent power) of average power of virtual electric energy consumption in electric network (active power) and U and I. However, 2 can be applied when voltage and current are standard sine signals only. If this condition cannot be satisfied, (2)electric network power measurement cannot be used. In the real electric network, signals of voltage and current almost are not sine signals which only include 50Hz frequency part. It includes a lot of signals, such as 100Hz, 150Hz, 200Hz and so on. These signals are called harmonic signal. In addition, electric network load, especially switch on-off of power supply also may cause all kinds of noise, voltage harmonic and distortion of waveform. If use (2) to conduct electric energy measurement, these "pollution signal" shall lead to serious error. As a result, modern electric energy measurement method is to calculate power and electric energy pass

electric energy meter according to the original definition of electric energy, namely (1).

In fact, we may discover that instantaneous power signal $P = ui$ is a signal includes direct current part and high frequency part. Any frequency part that frequency is not 0 has no contribution to integral of time in a long term. Thus, electric energy measurement equals calculating integral that direct current part of instantaneous power P to time in mathematics. This is principle that PL3000 series conduct active electric energy measurement.

Processing of Digital Signal of PL3223 active measurement

PL3223 uses six 16bit   type of ADC to convert analog signals of three routes voltage and current to digital signal. And conduct digital signal processing for gaining active power in chi. See PL3223 principle chart on page 1.

1. High-Pass Filter

PL3223 firstly conducts same high pass filter operation for six routes signal of voltage current inputted. This is because voltage current' AC signal shall lead direct current bias when conducting sampling, especially after OPA. Thus, we defines concept of error of power measurement. PL3223 uses six routes IIR digital high pass filer to erase direct current signals of voltage and current signals. The character of frequency response is shown in chart 4.
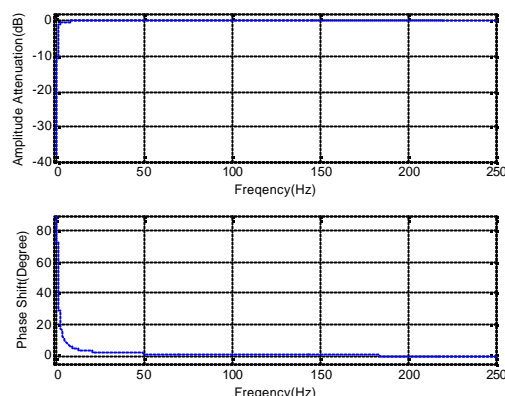

4 PL3223 HPF frequency domain response curve

One of the shortcomings of IIR type of filter is that filter has frequency response character of non-linear phase, namely the different frequency part of signals cause different delay of phase. Because PL3223 uses same IIR type of filter for voltage signal and current, it will generate same phase delay for the same frequency part of voltage and current signals. Thus the their   has no change, which do not affect integral of product of voltage and current. As we know, product of all of same frequency voltage and current is contributing to integral of time of total electric energy. Integral of product of different frequency voltage and current is 0. As a result, high pass filter of PL3223 will not generate any measurement error for the reason of phase error.

2. OFFSET

The power measurement is influenced by the signal coupling between phases in PCB or Chip. In order to avoid the affection, PL3223 supplies the function that register OFFSET   00 01H calibrate effect of coupling signals. The register usually does not need to be used. In real application, it is all configured as 0.

PL3223

3. Low Pass Filter

PL3223 conducts low-pass digital filter processing before integrating product signal of voltage and current. Its main purpose is to make only DC signal pass and reduce jitter of CF pulse output. For knowing about the affection that low-pass filter affects power accumulation, please see Figure 5.
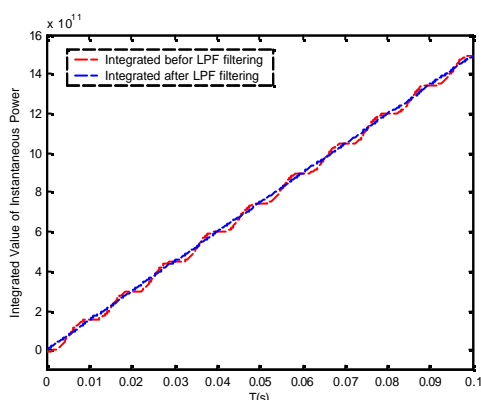

Figure 5 The affection that low-pass filter affects the power accumulation

4. Three-phase active measurement

The calculation of three-phase energy is to calculate the sum from active energy consumed by phase A, B and C respectively. However, virtual three-phase distributing network has two kinds of modes of connection. They are three-phase three-wire system(triangle/ connection) and three-phase four wire system star type/Y connection . The difference of the connection modes is the former does not supply zero wire which as neutral point. PL3223 can supply support for three-phase three-wire and three-phase four-wire connection modes. Through configuring TF pin voltage as 0 or 5V PL3223 shall be configured as three-phase four-wire or three-phase three-wire mode.

In the mode of three-phase four-wire, the formula of power measurement of PL3223 is:

$$P = U_a I_a + U_b I_b + U_c I_c \qquad (3)$$

In the mode of three-phase three-wire, the formula of power measurement of PL3223 is:

$$P = U_{ac} I_a + U_{bc} I_b \qquad (4)$$

In three-phase four-wire mode, the mutual-inductance signals of three-phase linear current are respectively placed into IAP, IAN, IBP, IBN, ICP and ICN. The common potential point of PT output links UN. Its another interface links UA   UB and Uc respectively. See figure 6.

In the mode of three-phase three-wire, the principle of power measurement of PL3223 equals to measuring power of figure 6. Thus, it is different to the connection of three-phase four-wire mode. The connection of three-phase three-wire mode may refer to connection way of this method. Configure linear voltage as UAB and UAC connect a terminal of joint point of two-way line PT to UN pin of PL3223; Connect other two terminals to UA and UB of PL3223. Link current mutual induction signal of IA and IB to pins IAP, IAN and IBP, IBN of PL3223. In three-phase three-wire mode, the voltage C and current access of PL3223 are automatically shielded. As a result, pins of UC, ICP and ICN may directly connect earth.

Notice: When calibrating three-phase three-wire system meter, some three-phase calibration system supplies current of phase A and phase C. For the meter needs to use this calibration system, we only need to exchange signal input of access B and access C in design. Namely, line voltages connected are U_{AB} U_{CB}. Measurement currents are line current signals from access A and access C. See figure 7.
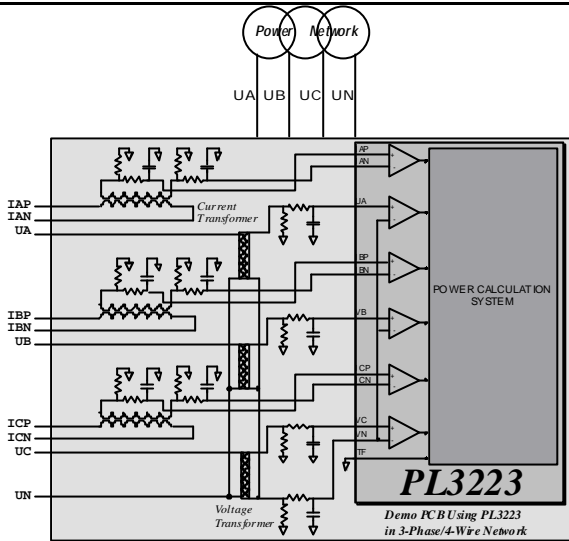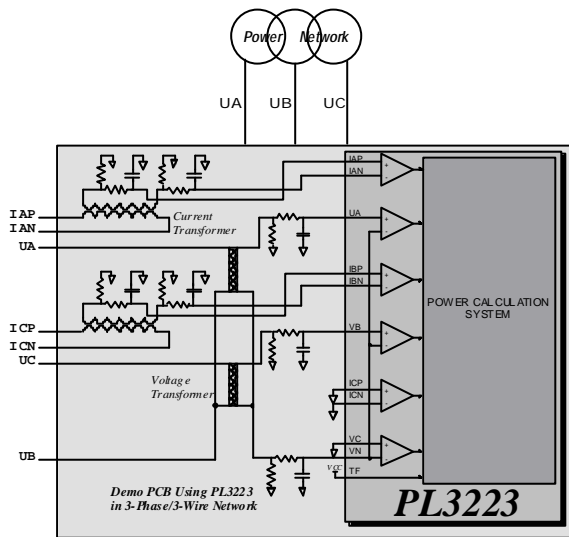
Figure 6 Wiring chart of three-phase four-wire system

Figure 7 Wiring chart of three-phase three-wire system

Phase Options

For the convenience that user respectively conducts power measurement calibration to every phase, PL3223 supplies phase option pins OS1 and OS2. The different level configuration of OS1, OS2 shall result power measurement pulse PCF, QCF and power symbol indication PDIR, QDIR respectively correspond to the different phase. The meaning of OS1 OS2 configuration is shown in the table below.

OS1	OS2	Corresponding Phase
0	0	Three-phase total power
0	1	Phase A
1	0	Phase B
1	1	Phase C

Symbol Indication

PL3223 supplies two pins PDIR and QDIR, which are respectively used to indicate the symbols of current active power and reactive power. If the angle between voltage signal and current signal is more than 90 degrees, probably because load terminal has electric generator or meter connection is reversed PDIR shall output high level indication.

Absolute Value Processing

In order to prevent meter's connection mistake or appearance of negative active power measurement which is resulted by baleful change, PL3223 supplies optional absolute value processing function. When configure pin MOD(31) as high level, PL3223 shall conducts absolute value processing for the signals each phase' product of voltage and current through low pass filter. Here, any angle degrees between voltage and current will not affect that active power is positive. Notice: If load includes electric generator, configuring absolute value processing will make electric energy measurement have heavy error. Thus, unless assuring there is no electric generator in load, —namely, stream of current network electric energy is always one direction, Do not configure MOD as high. In addition, reactive

measurement will not be affected by MOD. Because it is unimaginable that there is only positive reactive equipment is important and there is no negative active equipment is important in a network.

Phase Compensation

Design of modern meter and collection of voltage signal usually use voltage sensor method. Collection of current signals usually uses current sensor or manganin resistance voltage division method. However, any method cannot make phase delay of voltage and current completely same during connection. This will result quite big error of power measurement. Through configuring three digital phase calibration register DPCA(14), DPCB(15) and DPCC(16), PL3223 conducts compensation for phase difference during the period of signal sampling. DPCA, DPCB and DPCC are three 1byte registers, which configuring scope is from −31 to 31. Notice: negative configuring of DPC needs to be expressed by base-minus-one's complement, namely, use the first bit to express symbol（1 is negative）. The following seven bits express absolute value. Thus, the scope of available positive number is from 01 to 1F. The scope of input negative is from 81 to 9F. The phase scope（can be corrected is about between -0.93° and ~0.93° through adjusting）DPC. Configuring DPC as positive number, which will enlarge the phase angle between voltage of current phase and current of current phase, whereas, it will reduce phase angle. The method that adjusting DPC conducts calibration may refer to number calibration on page 10.

Creeping Stop Function

All kinds of electric energy meter standard

have exact rule for no-load output. For example, GB/T 17215 standard demands that test of meter should not output over one pulse when using voltage and there is no current in current circuitry. To startup current, meter can start up and continuously record when current is 0.004Ib. PL3223 supplies creeping configuring register, which may stop power pulse output less than startup current.

The principle of PL3223's creeping configuring register QDGATE（17H） is to make the biggest pulse interval. The calculation is shown as following

$$Max\ T_{CF} = QDGATE * 2^{16} / 5000\,(s) \qquad (5)$$

For example, if configure QDGATE as 1（all pulses output that pulse output time over 13.1 seconds far from last）pulse output will be stopped. Thus, for configuring creeping stop threshold, firstly we may work out pulse interval time when is corresponding to least startup current. Then, according to this least pulse interval and relational expression (5), we can work out configuring value of QDGATE.

If designing a electric energy meter which Ib（5A, pulse constant is 1600 imp/kwh） the design does not measure active power caused by the current less than 0.002Ib. Then, calculation of pulse output time interval of 0.002Ib current is

$3.6*10^6/(3*220*5*0.002*1600)=341$（second） bring it into (5) to get QDGATE（26） then configure QDGATE as 1A.

Reactive Measurement

According to definition of IEEE standard nomenclature dictionary 100, definition of reactive power in mathematics is

$$Q = \sum_{n=1}^{o} V_n \times I_n \times \sin(\mathbf{j}_n) \qquad (6)$$

V_n And I_n are RMS values of nth power harmonic signals of voltage and current. In practical application, usually there are three ways to measure reactive power. They are Delay method, Triangle method and 90-degree phase-moving method. The compare of their advantages is shown in the table below.

Method	Detail	Advantage	Disadvantage
Delay Method	Delay voltage signal till 1/4 cycle, and then multiply current by this voltage to accumulate.	The method is simple	Only can be used for fixed frequency ; There is big error when frequency has deviation or harmonic.
Power Triangle Method	Calculating apparent power according to RMS value ; Utilizing power triangle relation to calculate reactive power	It is suitable for 50Hz electric network and 60Hz electric network	It is only suitable for standard sine signals of voltage and current. There is bigger error when there is harmonic.
90degree phase -moving method	Make voltage signal pass a 90 degree Hilbert phase-moving filter, and then multiply current signal by this voltage signal. To accumulate.	Strict implementing according to the definition of reactive power. It is suitable to all kinds of frequency and voltage/current signals which include harmonic.	Adopt Hilbert filter, so that increase complicacy of design.

PL3223 uses 90-degree phase-moving method to calculate reactive power and reactive energy.

PL3223 has three built-in Hilbert FIR filters. Which conduct 90 degrees phase-moving filtering for three-phase voltage A B and C respectively. After completing 90 degrees phase-moving filtering, using these voltage signal and current signal to calculate reactive power through the method of multiplying—filtering—accumulating,which is completely same to calculating active power. Hilbert that PL3223 realizes is FIR(limited pulse excitation response)type filter which has strict linearity phase see Figure 8 PL3223 also solves delay problem of fractional-class sampling time of Hilbert FIR filter. For harmonic voltage of all kinds of frequency, it always conducts precise phase-moving of 90 degrees. As a result, PL3223 can supply reactive power measurement of up to 21 times harmonic precisely.
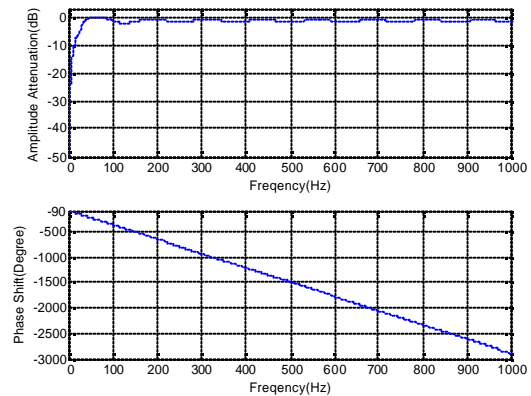

Figure 8 Frequency domain response of Hilbert filter

Digital calibration of meter

PL3223 supports digital power calibration, because PL3223 provides configurations of 13 registers in all. These registers include pulse output active pulse threshold GATE three-phase active/reactive gain calibration GAIN active/reactive OFFSET, and digital phase calibration DPC. As a result, in the practical application, we have the method of digital calibration of meter through setting register except the traditional calibration method of resistance and capacitance of

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adjusting PCB board.

PL3223 continuously implement accumulation operation of product of voltage and current, and check the compare value between current accumulation value and settled pulse output threshold GATE. Once accumulation value over GATE, it outputs a pulse and implement new accumulation. Thus, continuous adjusting of proper pulse output threshold can make frequency of output pulse comply with calibration standard. However, it exists another problem. Because there is a little dfference between components of PCB board and three-phase voltage and current ADC, transformation ratio of three-phase voltage and current A, B, C is not completely same. As a result, the adjusted GATE value according to phase A probably is not suitable for phases B and C. Similarly, reactive measurement also exists the same problem.

In order to solve the problem, PL3223 supplies six gain correction registers. They are PGAINA(04~05H), PGAINB(06~07H), PGAINC(08~09H), QGAINA(0E~0FH), QGAINB(10~11H), and QGAINC(12~13H), which are used to adjust difference of transformation ratio between each phase in active/reactive measurement. The correction function of register GAIN in power measurement may be expressed by following formula

$$P_{GAIN} = P \times 1 \quad \frac{GAIN}{2^{16}})$$ (7)

Thus, the range that GAIN adjusts power is between 0 and double. This is enough.

Take the example of active measurement correction, the digital calibration procedure of PL3223 is shown as following:

1. Order power factor=1 and set OS1=01, OS2=01 or order phases B and C are unloaded through setting meter calibrating

system. Here, active power pulse outputs power of phase A.

2. Adjusting GATEP to make pulse output comply with calibration standard.

3. Set OS1=10 and OS2=10, or order phases A and C are unloaded. Here, active power pulse outputs power of phase B.

4. Adjusting PGAINB to make pulse output comply with calibration standard.

5. Set OS1=11 and OS2=11, or order phases A and B are unloaded. Here, active power pulse outputs power of phase C.

6. Adjusting PGAINC to make pulse output comply with calibration standard.

7. Adjust power factor to be 0.5, and set OS1=01, OS2=01; or order phases B and C to be unloaded. Adjusting DPCA to make pulse output comply with calibration standard

8. Adjusting power factor to be 1. Adjusting PGAINA to make pulse output comply with calibration standard

9. Repeat 7 and 8 for a few times, which make pulse output of phase A comply with calibration standard in any cases of power factors

10. Use the method similar to 7,8,9 to adjust phases B and C which make pulse output of phases B and C comply with calibration standard in any cases of power factors

11. Here, calibration of active measurement has been completed.

We can use similar method to calibrate for reactive measurement. Digital calibration of meter has the following advantages: calibration speed is fast; correction precision is high; and PCB does not need to be changed. Combining with standard energy meter with digital interface, correction system can realize high effective automatic calibration of meter.

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Resistance network calibration

PL3223 supports resistance network calibration. Through simple adjusting of resistance of voltage sampling, we can calibrate meter.

1. Illumination of parameter configuration
When we use inside benchmark source of PL3223, PGA is 4 times gain, and exterior current/voltage power factor is 1 frequency of three-phase four-wire active pulse CF may be estimated approximately according to the following formula.

$$CF=3*192.94*Vu*Vi/CFSCL \qquad (7)$$

Word wheel drive pulse frequency (namely, pulse frequency of F1 or F2 pin) estimation formula is

$$F=3*192.94*Vu*Vi/CFSCL/FSCL \quad (8)$$

Notice : here, Vu is RMS value of voltage difference signal from pin UA, UB, UC and UN ; unit is Volt(V), Vi is RMS value of current difference signal from pins IAP and IAN, IBP and IBN, ICP and ICN, unit is Ampere(A). In this formula, CFSCL, FSCL are determined by level from SCF, S2 and S1. It is shown in the table below :

SCF	S2	S1	CFSCL	FSCL
0	0	0	1	32
0	0	1	2	32
0	1	0	4	32
0	1	1	8	32
1	0	0	4	8
1	0	1	8	8
1	1	0	16	8
1	1	1	32	8

Take an example for explanation:
Set PGA to be 4 times gain, do not change configuration of inside register, in the case of rated current, the RMS value of difference input signal of three-phase voltage/current are Vu=200mV, Vi=50mV approximately. Through configuring different SCF/S1/S2, we can respectively obtain the corresponding CF frequency. It is shown in the table below:

SCF	S2	S1	CFSCL	FSCL	CF(Hz)
0	0	0	1	32	5.79
0	0	1	2	32	2.89
0	1	0	4	32	1.45
0	1	1	8	32	0.72
1	0	0	4	8	1.45
1	0	1	8	8	0.72
1	1	0	16	8	0.36
1	1	1	32	8	0.18

2. Frequency choice of meter design
When we use PL3223 to design three-phase meter, we should firstly work out rated output frequency of CF according to designed rated voltage value Un(unit:Volt), rated current value Ib(unit:Ampere) and selected pulse constant N (unit:imp/kWhr), such as three-phase four-wire meter which can reffer to the following formula:

$$CF=3*Un*Ib*N/3600000 \qquad (9)$$

Notice: this formula is only suitable for three-phase four-wire meter. Un usually adopts RMS value of actual phase voltage such as 220V. For three-phase three-wire meter, in fact we measures voltage and current of two ways. So, we need to adjust this formula.

$$CF=2*Un*Ib*N/3600000 \qquad (10)$$

Here, Un adopts RMS value of line voltage, such as 100V or 380V.
According to CF frequency has been worked out, selected word-wheel transformation ratio type, and formula (7),(8), we can select proper status from SCF S2 and S1 by calculating.

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Held an example for explanation : We want to design a three-phase energy meter. Its rated voltage is 220V rated current is 5A pulse constant is 800imp/kWhr word-wheel choice is 200 :1. Firstly, we need to adjust transformation ratio relationship of voltage and current signals through designing the value of capacitance and resistance of board, which make the RMS value of difference input signal of pin voltage and pin current of PL3223 chip be about 200mV and 50mV in the case of rated voltage and current. According to formula (9), rated output frequency of CF is :

3*220*5*800/3600000=0.7333Hz

According to formula (7) or table of the example above, when SCF/S2/S1 are set as 011 or 101, CF output is :

3*192.94*0.2*0.05/4=0.72Hz

It is most close to the rated CF output frequency worked out above. In addition, pulse constant is 800, namely, 800 pulses represent 1 degree electricity ; word wheel is 200 :1, namely, when F1 and F2 are inputed 100 pulses, dial steps 1 degree electricity. And FSCL equals to the pulse that CF pulse is divided frequency on pins F1 and F2. Thus, FSCL should be set as 8, namely make CF pulse be 8 frequency divisions. SCF/S2/S1 should be set as 101. This confifuration is most close to nicety value, which benefit meter calibrating.

Function of word-wheel drive

PL3223 supports output of two-phase two-beat word-wheel counter drive, which use pin F1, F2, F3 and F4. Thereinto, F1 and F2 are output of active word-wheel counterdrive; F3 and F4 are output of reactive word-wheel counter drive.

F1/F2(F3/F4) alternately generate negative pulse. The negative pulse'width is 275ms. The

time Between the falling edge of F1(F3) and the falling edge of F2(F4) is approximate half cycle of F1(F3). When cycle of F1(F3),F2(F4) is less than 550ms, negative pulse width of F1(F3),F2(F4) is half cycle. See the table below.

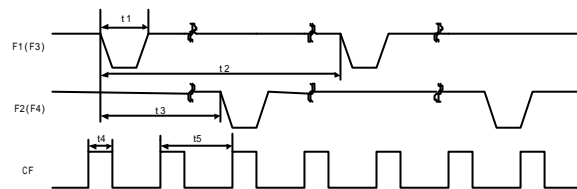| Parameter	Unit	Description
t1	275ms	F1,F2,F3,F4 negative phase pulse width
t2		F1,F2,F3,F4 output pulse cycle
t3	1/2 t2	Time that from falling edge of F1(F3) to falling edge of F2(F4)
t4	100ms	CF positive phase pulse width
t5		CF output pulse cycle

Figure 9 Sequential chart of word-wheel counter frequency output

## Function of temperature compensation

PL3223 embeds temperature frequency changer. Frequency output of temperature frequency changer will change with changes of chip temperature. When temperature sensor is enabled, inside frequency-timing counter accumulates times of output frequency of temperature frequency changer at cycle of 20ms. The final accumulation time is sent into temperature frequency register (2AH,2BH). The numerical value of temperature frequency register updates once every 20ms. MCU reads numerical value of temperature frequency

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register to obtain information of current temperature change through SPI serial interface. Then, it is correspondingly processed by software. The following figure is the compare table between temperature and temperature frequency register:

Asdf

Compare table of temperature and temperature frequency
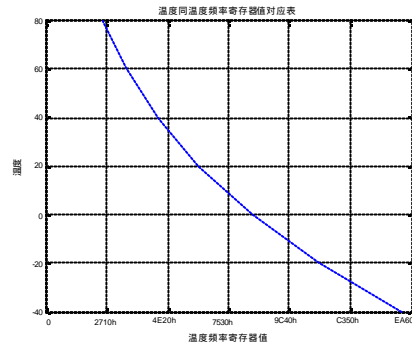
Temperature frequency register value

Figure 10 Character curve of temperature sensor

SPI Serial Interface

PL3223 embeds SPI serial interface. This serial interface has 4 signal terminals. They are CS, SCK, SI, and SO. SCK is that serial clock passes input terminal; SCK is that data is inputted to SI terminal at leading edge; When SCK is at falling edge, data outputs from SO; CS is chip select input. This input terminal is used in the situation that few parts use one serial bus together. The falling edge of CS is resetting signal of serial interface. Serial interface' inside logic initialization. When CS is at low level, PL3223 enters communication mode. During the period of whole procedure of data transmission, CS is always low level. If CS is high during data transmission, this data transmission is failed, and serial bus turns to be high-impedance status. If there is only a PL3223 part on serial bus, CS is always low level.

Notice After CS is constant low, reading address or writing address have to be continuously increased. If we want to write two discontinuous addresses, we have to conduct operation of pull-up resetting every time for CS.

Visit of all special function registers of PL3223 is realized through SPI serial interface. They may update data or read data. After CS is low level, PL3223 enters communication mode. In communication mode, firstly write communication command-word to communication command-word register, which includes register address and appointment of reading/writing operation of next data transmission. Thus, no matter reading operation or writing operation, all data transmission operations of PL3223 have to firstly write communication command-word.
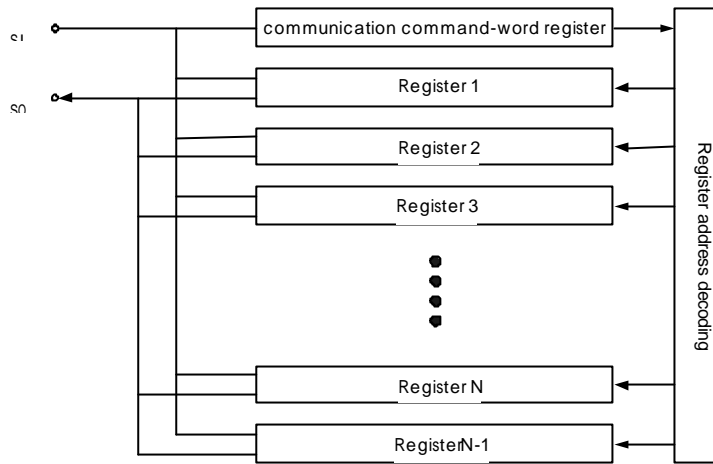
Figure 11 PL3223 addresses through communication command-word register

Communication command-word register is an 8-bit write-only register. The highest bit is used to confirm that next data transmission operation is reading mode or writing mode. The low 6-bit is address register visits. Figure 12 and Figure 13 are sequential charts completing once reading/writing operation of data transmission.
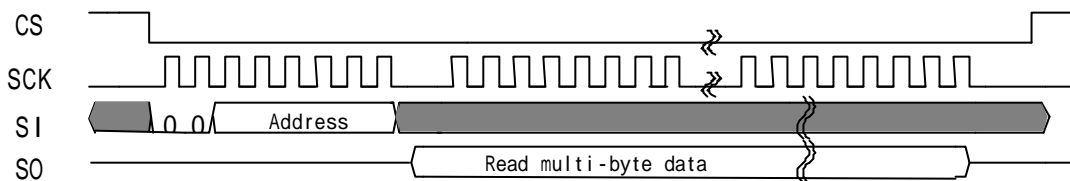

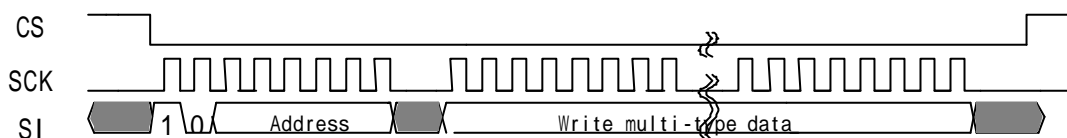Figure 12 Read data from PL3223 through SPI interface

Figure 13 Write data to PL3223 through SPI interface

SPI writing operation

When CS of PL3223 is low level, it is in communication mode. The first byte is written into writing communication command-word register. The highest bit of this register has to be written as 1, which express data transfer later is used to write into inside register of PL3223. The low 6-bit of this byte expresses address written into register. PL3223 starts to move data into register at leading edge of SCK. When CS is high level, writing operation of data is invalid. When a byte of data is fully moved into corresponding register of PL3223, inside address indicator will automatically plus 1, and points to next register address. Thus, it can continuously write few registers. And it does not need to repeat writing communication command-word register.

Notice: Registers of PL3223 have write protection function. Before conducting writing operation,

write protection has to be removed. The method is to write a byte FF of data to address 3F and write a byte 00 of data to address 3F to make write protection be valid.
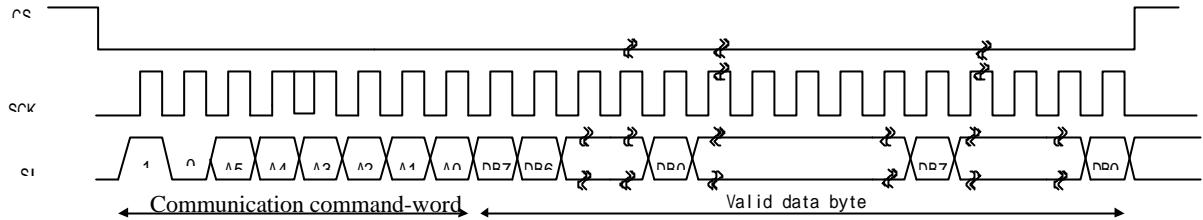

Figure 14 Write Sequential of SPI Interface

SPI Read operation

CPU reads data from PL3223 through serial interface, Data is between falling edge output of SCK and SO port. According to write operation method mentioned above, it is necessary to write communication command-word before reading data. When CS is low level, PL3223 enters communication mode. It needs to write 8-bit data to communication command-word register. The highest bit has to be 0, which express the latter operation is read operation. The low six-bit is register address whose data is read. PL3223 starts to move out data at falling edge of SCK. SO turns to data from high impendence and output to bus. After CS becomes high level, read operation is invalid. SO turns to high impendence again. After one byte of data is completely output, the address indicator of built-in register of PL3223 adds 1 automatically and points to next address of register. It can continuously read many registers and does not need to repeat write communication command-word.
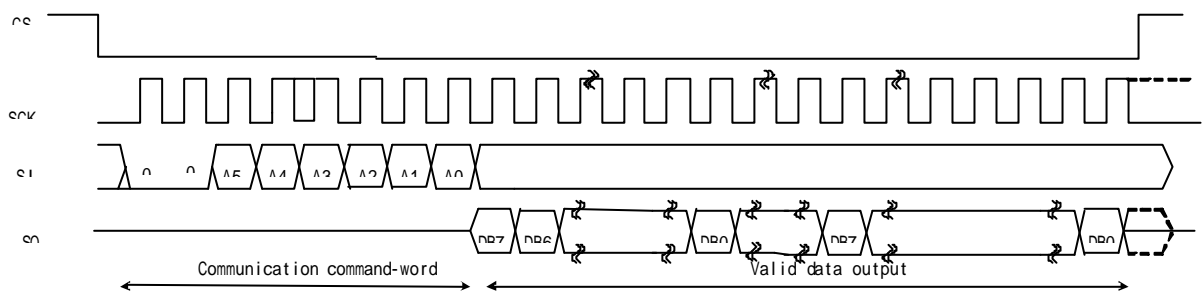
Figure 15 Read Sequential of SPI Interface

Interrupt

PL3223 interrupt marks happening of over-voltage or under-voltage. PL3223 interrupt is managed through interrupt control register(1BH) and interrupt status register(29H). When PL3223 occurs interrupt, the corresponding zone bit is set as 1 in interrupt status register. If control bit of this interrupt is also set as 1 in interrupt control register, pin INT outputs low level. Status of Interrupt status register zone bit is not relative to control bit of interrupt control register. For the detailed content, please see "interrupt register".

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Interrupt Application of MCU

Figure 16 displays basic operation application of MCU for PL3223 interrupt. INT is low level, which express one or more interrupts happen. Negative pulse edge that INT outputs will trigger exterior interrupt of MCU. When MCU detects one negative pulse edge, it executes Interrupt Service Routine (ISR). Exterior interrupt mark will be eliminated during executing ISR. MCU reads content of interrupt status register for confirming interrupt source, so that it can conduct corresponding detailed processing. After completing of processing, interrupt returns.

Interrupt Sequence

The pin INT of PL3223 is used to indicate voltage over over/under valve value. INT is always high level if there is no interrupt. After interrupt happens, INT turns to low level from high level, namely it generates negative pulse. Pulse width is 1.5ms, which is the respondent time of MCU. Whether MCU responds or not responds interrupt, pin INT will be pulled up again. If there is other accidents are happening at the same time, PL3223 generates interrupt again. Pin INT will be low level and waiting for respondence interrupt of MCU. During INT is low level, if there are any new interrupts, it will not produce new interrupt again and only can inquire the status of interrupt status register.
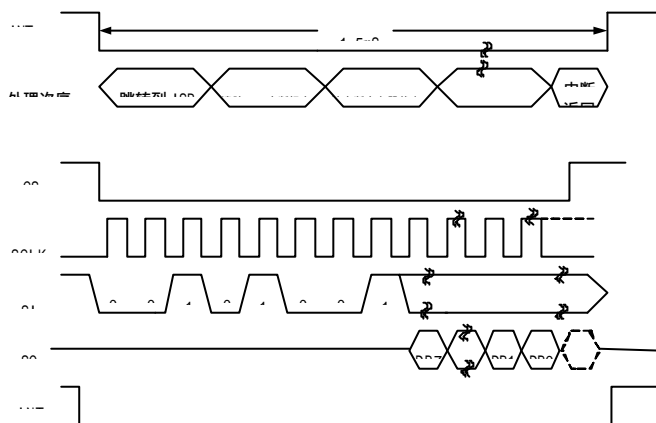
Figure 13 Sequence that SPI reads interrupt register

Visit of register of PL3223 chip

All functions of PL3223 are realized through visiting corresponding register of this chip. All visits for every register are realized through SPI serial interface. For relevant agreement of serial interface, please see part" serial interface" .

SPI control register

It is a [7:0] bit write-only register, which control serial data transmission between PL3223 and main processor. All operations of data transmission have to first implement write operation to SPI control register. This data determines that next operation is read operation or writing operation And determines which register will be operated correspondingly.

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Bit	Mnemonic symbol	Description
0 5	A0 A5	Define register address that correspond to data transmission operation See table [7:0] for detailed definition.
6	Reserved	This bit is not set. It is expressed as 0.
7	W/R	This bit is 1, which express conducting write operation for corresponding register address This bit is 0, which express conducting read operation for corresponding register address.

For details of every bit, please see the table below:

D7	D6	D5	D4	D3	D2	D1	D0
W/R	0	A5	A4	A3	A2	A1	A0

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Appendix　　Register list of PL3223

Address	Name	Read/write	Valid bit	Default	Description
01h~00h	P_OFFSET	W/R	[15:0]	0	Double-byte active energy compensation value, have symbolic number. It is used to compensate or counteract additional active energy caused by the system in the procedure of active measurement. Usually, it does not need to be configured.
03h~02h	P_GATE	W/R	[15:0]	5FFFh	Double-byte active energy measurement threshold　have not symbolic number. The function is to adjust measurement precision of energy in the procedure of calibration. When accumulation amount of energy over this threshold, calibration pulse PCF is produced. Obviously, this threshold is more small, appearance frequency of calibration pulse PCF is more high, whereas, appearance frequency of calibration pulse PCF is more low.
05h~04h	PA_GAIN	W/R	[15:0]	0	Double-byte phase A active measurement gain minitrim register. have symbolic number. This chip adopts three-way same circuit structure to respectively conduct sampling process of three-phase energy. Because the three phases adopt same energy measurement threshold and there is always a little difference among sampling processes of the three phases in practical systme application, we need to compensate the measurement error caused by asymmetry of system through setting this register as rational value. The result is: energy that three phases are completely same or anyone phase energy respectively conduct calculation through three ways. The measurement result must be completely same.
07h~06h	PB_GAIN	W/R	[15:0]	0	Double-byte phase B active measurement gain minitrim register, have symbolic number. The detailed illumination is same to

					pA_gain.
09~08h	PC_GAIN	W/R	[15:0]	0	Double-byte phase C active measurement gain minitrim register, have symbolic number. The detailed illumination is same to pA_gain.
0bh~0ah	Q_OFFSET	W/R	[15:0]	0	Double-byte reactive energy compensation value, have symbolic number. It is used to compensate or counteract additional reactive energy caused by the system in the procedure of reactive measurement. Usually, it does not need to be configured.
0d~0ch	Q_GATE	W/R	[15:0]	5FFFh	Double-byte reactive energy measurement threshold have not symbolic number. The function is to adjust measurement precision of energy in the procedure of calibration. When accumulation amount of energy over this threshold, calibration pulse QCF is produced. Obviously, this threshold is more small, appearance frequency of calibration pulse QCF is more high, whereas, appearance frequency of calibration pulse QCF is more low.
0f~0eh	QA_GAIN	W/R	[15:0]	0	Double-byte phase A reactive measurement gain minitrim register, have symbolic number. The detailed illumination is same to pA_gain.
11h~10h	QB_GAIN	W/R	[15:0]	0	Double-byte phase B reactive measurement gain minitrim register, have symbolic number. The detailed illumination is same to pA_gain.
13h~12h	QC_GAIN	W/R	[15:0]	0	Double-byte phase C reactive measurement gain minitrim register, have symbolic number. The detailed illumination is same to pA_gain.
14h	DPCA	W/R	[7] [5:0]	0	Single-byte phase A digital phase correction register, base-minus-one's complement. For details, please see section" phase compensation" .
15h	DPCB	W/R	[7] [5:0]	0	Single-byte phase B digital phase correction register base-minus-one's complement. For details, please see section" phase

					compensation″.
16h	DPCC	W/R	[7] [5:0]	0	Single-byte phase C digital phase correction register, base-minus-one's complement. For details, please see section″ phase compensation″.
17h	QD_GAT E	W/R	[7:0]	0	Single-byte creeping threshold have no symbolic number. When power is less than this value, it does not implement energy measurement. When qd_gate=0 creeping function is invalid.
18h	PEAK_G ATE	W/R	[7:0]	7Fh	Single-byte overvoltage detecting threshold, have no symbolic number. In the procedure of continuous sampling of line voltage, once voltage value over this threshold, it is approved that corresponding line is in overvoltage status. The corresponding bit of int_ena determines whether interrupt is produced.
19h	SAG_GA TE	W/R	[7:0]	0	Single-byte under-voltage detecting threshold, have no symbolic number. When line voltage value is less than this detecting threshold, the line is in under-voltage status. If line voltage values do not over this threshold in continuous many half-cycles, the corresponding bit of int_ena determines whether producing interrupt. For details, please see section ″ int_ena register explanation″. Detecting cycle number is determined by sag_p.
1Ah	SAG_P	W/R	[7:0]	FFh	Single-byte under-voltage half cycle mumber have no symbolic number. For producing interrupt, design needs to make half cycle mumber that under-voltage status has to retain at least.
1Bh	INT_EN A	W/R	[6:4] [2:0]	0	Voltage detecting interrupt enable register, Meanings that each bit represents, for the detail, please see section ″ int_ena register explanation″.

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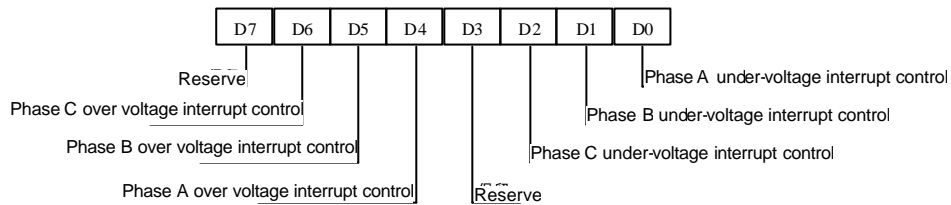| 1Ch	SEL_CH	W/R	[1:0]	1	Three-phase channel-choice control register, which is used to select anyone phase of the three phases to conduct measurement of RMS value of line voltage frequency, current and voltage. sel_ch 1 means to select phase A sel_ch 2 means to select phase B sel_ch 3 means to select phase C.
1Dh	TS_ENA	W/R	[0]	0	Temperature sensor enable
20h	PA_CNT	R	[7:0]	0	Single-byte phase A active energy mesurement pulse counter no symbol.
21h	PB_CNT	R	[7:0]	0	Single-byte phase B active energy mesurement pulse counter no symbol.
22h	PC_CNT	R	[7:0]	0	Single-byte phase C active energy mesurement pulse counter no symbol.
23h	PS_CNT	R	[7:0]	0	Single-byte combined phase active energy mesurement pulse counter no symbol.
24h	QA_CNT	R	[7:0]	0	Single-byte phase A reactive energy mesurement pulse counter no symbol.
25h	QB_CNT	R	[7:0]	0	Single-byte phase B reactive energy mesurement pulse counter no symbol.
26h	QC_CNT	R	[7:0]	0	Single-byte phase C reactive energy mesurement pulse counter no symbol.
27h	QS_CNT	R	[7:0]	0	Single-byte phase-merger reactive energy mesurement pulse counter no symbol.
28h	DIR	R	[7:0]	0	Energy symbol indication mark of three-phase channel. For the detail, please see section" dir register explanation".
29h	FLAG	R	[6:4] [2:0]	0	Over/under voltage indication mark of three-phase channel. For the detail, please see section" flag register explanation".
2Bh~2Ah	TS_CNT	R	[15:0]	0	Double-byte temperature sensor counter no symbol.
2D~2CH	ADU	R	[15 :0]	-	Sampling data of voltage real-time waveform expressed by two-byte symbolic number. SEL_CH selects which phase needs to be changed in. Update is conducted at falling edge of pin CONVERT. For the detail, please see section'AD user interface of 3223'.

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Address	Name	R/W	Bits	Default	Description
2F~2EH	ADI	R	[15 :0]	-	Sampling data of current real-time waveform expressed by two-byte symbolic number. SEL_CH selects phase needs to be switched to Update is conducted at falling edge of pin CONVERT. For the detail, please see section'AD user interface of 3223'.
31h~30h	DFC	R	[15:0]	0	Double-byte frequency measurement register, no symbol. For the detail, please see section" dfc register instruction" .
33h~32h	PEAK	R	[15:0]	0	Double-byte nominal voltage peak value register, no symbol. According to this register, we may calculate overvoltage and under voltage threshold. When it Implements once write operation in register that address is 30h, calculation of nominal voltage peak value is startted up. The value of this register will be renovated after the time of one cycle.
37h~34h	VRMS	R	[31:0]	0	Four-byte voltage square integrate value no symbolic number. It is used to calculate RMS value of voltage. For the detail, please see section" measurement of RMS value of voltage and current " .
3Bh~38h	IRMS	R	[31:0]	0	Four-byte current square integrate value no symbolic number. It is used to calculate RMS value of current. For the detail, please see section" measurement of RMS value of voltage and current " .
3Dh~3Ch	M_CNT	R	[15:0]	0	Number of sampling point in the process of calculating average voltage and average current. It is used to calculate RMS value of current. For the detail, please see section " measurement of RMS value of voltage and current " .

Appendix   Instruction of Special Registers

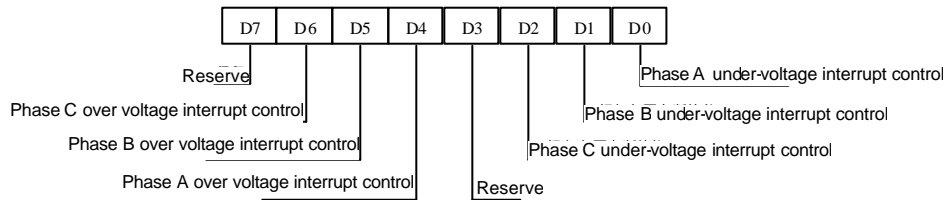### Explanation of DPC Register

Setting this register is for eliminating phase error caused by system and avoiding different measurement precision in the case of different phase. DPCA [7] expresses direction of movement. when DPCA [7]=1 voltage moves left; when DPCA [7]=0 voltage moves right. DPCA [5:0] expresses movement degree. In addition, movement degree and value of DPCA [5:0] are direct proportion. The maximum movable value is about 0.1 degree (when DPCA [5:0]   3FH).
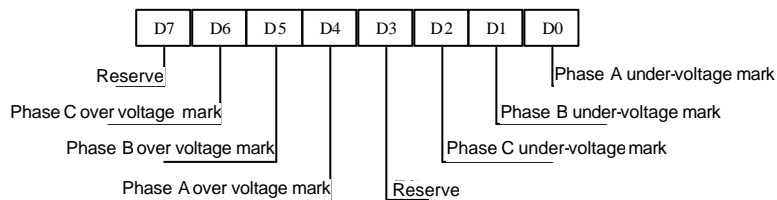
Explanation of INT_ENA Register

D7	D6	D5	D4	D3	D2	D1	D0

Reserve

Phase C over voltage interrupt control

Phase B over voltage interrupt control

Phase A over voltage interrupt control

Reserve

Phase A under-voltage interrupt control

Phase B under-voltage interrupt control

Phase C under-voltage interrupt control

Notice   All bits are valid when they are high.

Explanation of DIR Register

D7	D6	D5	D4	D3	D2	D1	D0

Reserve

Phase C over voltage interrupt control

Phase B over voltage interrupt control

Phase A over voltage interrupt control

Reserve

Phase A under-voltage interrupt control

Phase B under-voltage interrupt control

Phase C under-voltage interrupt control

Notice   If bit is high, it expresses negative power   If bit is low, it expresses positive power.

Explanation of FLAG Register

D7	D6	D5	D4	D3	D2	D1	D0

Reserve

Phase C over voltage mark

Phase B over voltage mark

Phase A over voltage mark

Reserve

Phase A under-voltage mark

Phase B under-voltage mark

Phase C under-voltage mark

Notice   All bits are valid when they are high.

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Instruction of DFC Register

After implementing once write operation in the register which address is 3XH, calculation of line voltage frequency is started for once. User can read value of the register after 1 second.

actual frequency　$(250000\times OSC)/(dfc\times 9.6\times 10^{6})$.

Instruction of rms and M_cnt Register

After implementing once write operation in the register which address is 3Xh, calculation of average voltage and average current are started for once. After starting 300ms, user can read a group of 32BIT data from this register. The data are sampling value of current voltage. Extracting the square root of the data get measurement value of voltage Ub and sampling point number of voltage/current measurement Db. Because there is difference among systems, every system has to firstly read spot of this register before calculating voltage. Namely, After 300ms of starting voltage and current measurement in the case of 220V(rated voltage), reading the data of voltage meter and extracting the square root of the data to get Ua and sampling point number of voltage/current measurement Da. They are nominal value of 220V. Make current measurement value obtained and nominal value be proportion to obtain a multiple value of 220V. According to these values, we can work out current RMS value of voltage. The detailed formula is: $U_X=(Ub/Ua)\times 220\times (Da/Db)$

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Appendix   Specification

12.00±0.20 SQ
(.472±.004)

10.00±0.10 SQ
(.394±.004)

INDEX

0.80(.0315)
TYP

0.35±0.10
(.015±.004)

⌖ 0.16(.006)

1.50 .020 .010
(.059 .008 .004)

STAND OFF

0.10±0.10
(.004±.004)

8.00(.315)
REF

11.00(.433)
NOM

0.127 .005 .002
(.005 .002 .001)